CLAIMS

What is claimed is:

1. A method to efficiently design and implement a matched instruction set processor system, including:

decomposing the matched instruction set processor system into interconnected design vectors, each of the interconnected design vectors including a binding header method, a run method, a conjugate virtual machine (CVM), a binding trailer method, and an invocation method; and

analyzing and mapping the interconnected design vectors into a re-configurable platform.

2. The method of claim 1, wherein analyzing and mapping the interconnected design vectors includes:

mapping the interconnected design vectors into a pre-synthesis re-configurable platform.

3. The method of claim 2, wherein analyzing and mapping the interconnected design vectors includes:

transforming the pre-synthesis re-configurable platform into actual hardware through a physical realization process.

4. The method of claim 1, wherein analyzing and mapping the interconnected design vectors includes:

mapping the interconnected design vectors into a post-synthesis re-configurable platform.

5. The method of claim 4, wherein mapping the interconnected design vectors includes:

configuring the post-synthesis re-configurable platform at compile-time to match processing requirements of specific applications.

6. The method of claim 5, wherein configuring the post-synthesis re-configurable platform at compile-time includes:

using the CVM of each interconnected design vector to specify required attributes and capabilities; and

configuring the post-synthesis re-configurable platform at compile-time to match the required attributes.

7. The method of claim 6, wherein configuring the post-synthesis re-configurable platform at compile-time includes:

using the CVM of each interconnected design vector to specify required attributes; and

configuring the post-synthesis re-configurable platform at compile-time to match the required attributes.

8. The method of claim 7, wherein configuring the post-synthesis re-configurable platform at compile-time includes:

using the CVM of each interconnected design vector to specify required attributes, the required attributes including logic, placement, and routing information; and

configuring the post-synthesis re-configurable platform at compile-time to match the required attributes.

9. The method of claim 4, wherein mapping the interconnected design vectors includes:

configuring the post-synthesis re-configurable platform at run-time to match processing requirements of specific applications.

10. The method of claim 9, wherein configuring the post-synthesis re-configurable platform at run-time includes:

using the CVM of each interconnected design vector to specify required attributes; and

configuring the post-synthesis re-configurable platform at run-time to match the required attributes.

11. The method of claim 10, wherein configuring the post-synthesis re-configurable platform at compile-time includes:

using the CVM of each interconnected design vector to specify required attributes, the required attributes including a set of re-programmable parameters having values that can be downloaded and changed at run-time; and

configuring the post-synthesis re-configurable platform at compile-time to match the required attributes.

12. A system to efficiently design and implement a matched instruction set processor system, including:

an architectural modeling unit to decompose the matched instruction set processor system into interconnected design vectors, each of the interconnected design vectors including a binding header method, a run method, a conjugate virtual machine (CVM), a binding trailer method, and an invocation method; and

a realization mapping unit operatively coupled to the architectural unit to analyze and map the interconnected design vectors into a re-configurable platform.

13. The system of claim 12, wherein the realization mapping unit maps the interconnected design vectors into a pre-synthesis re-configurable platform.

14. The system of claim 13, wherein the realization mapping unit transforms the pre-synthesis re-configurable platform into actual hardware through a physical realization process.

15. The system of claim 12, wherein the realization mapping unit maps the interconnected design vectors into a post-synthesis re-configurable platform.

16. The system of claim 15, wherein the realization mapping unit configures the post-synthesis re-configurable platform at compile-time to match processing requirements of specific applications.

17. The system of claim 16, wherein the realization mapping unit uses the CVM of each interconnected design vector to specify required attributes and capabilities, and the realization mapping unit configures the post-synthesis re-configurable platform at compile-time to match the required attributes.

18. The system of claim 16, wherein the realization mapping unit uses the CVM of each interconnected design vector to specify required attributes, and the realization mapping unit configures of the post-synthesis re-configurable platform at compile-time to match the required attributes.

19. The system of claim 17, wherein the realization mapping unit uses the CVM of each interconnected design vector to specify required attributes, the required attributes including logic, placement, and routing information, the realization mapping unit configures of the post-synthesis re-configurable platform at compile-time to match the required attributes.

20. The system of claim 15, wherein the realization mapping unit configures the post-synthesis re-configurable platform at run-time to match processing requirements of specific applications.

21. The system of claim 20, wherein the realization mapping unit uses the CVM of each interconnected design vector to specify required attributes, and configures the post-synthesis re-configurable platform at run-time to match the required attributes.

22. The system of claim 21, wherein the realization mapping unit uses the CVM of each interconnected design vector to specify required attributes, the required attributes including a set of re-programmable parameters having values that can be downloaded and changed at run-time, and the realization mapping unit configures the post-synthesis re-configurable platform at compile-time to match the required attributes.

23. A machine-readable medium comprising instructions which, when executed by a machine, cause the machine to perform operations comprising:

decomposing the matched instruction set processor system into interconnected design vectors, each of the interconnected design vectors including a binding header method, a run method, a conjugate virtual machine (CVM), a binding trailer method, and an invocation method; and

analyzing and mapping the interconnected design vectors into a re-configurable platform.